IN THE SPECIFICATION

Please replace paragraph [0007] with the following paragraph:

[0007] The settling time for phase locked loops are mostly dependent upon the loop's bandwidth, which may vary greatly depending upon the specific application. Narrow band phase locked loops will have relatively ~~short~~ long settling time and correspondingly ~~short~~ long delay times between VCO activation and lock monitoring, whereas wider band loops will exhibit relatively shorter ~~longer~~ settling times and require a shorter ~~longer~~ delay period between VCO activation and lock check. As a consequence of the difference in required delay times, the conventional approach has been to build different phase locked loops for different loop bandwidths. As phase locked loops are highly integrated, it would be more advantageous to build a single system which could be used with application having differing loop bandwidth requirements.

Please replace paragraph [0031] with the following paragraph:

[0031] Subsequently at 306, a determination is made as to whether the selected tuning range results in a locked condition, indicating that the predefined frequency has been tuned to. As described above, the process in one embodiment includes activating the tuning circuit to tune to the predefined frequency, waiting a predetermined settling time and detecting a locked or unlocked condition of the phase locked loop. If a locked condition is not indicated, the process repeats 304 and 306 for another of the tuning ranges within the subset. In the above exemplary embodiment, the third tuning range is selected and its lock condition is checked to determine lock. In this manner, only two of the three VCOs are checked for lock, and accordingly the settling time for the phase locked loop is decreased. In the illustrated embodiment of the control circuit shown in Fig 1 and in the condition in which tuning range selection of all subset tuning ranges does not result in the detection of lock, the processes 304 and 306 continue repeating ~~one or more times~~ in order to permit the phase lock loop to continue ~~to~~ its search for a locked condition when the system experiences a temporary ~~abnormality~~ unlocked condition.